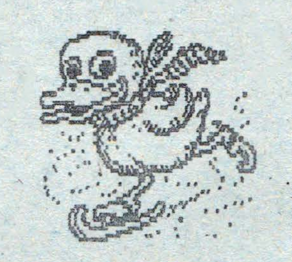


# MEMENTO TIMING Z-80



**ALPHA Ltd. @ 1991**

Tipografia MIRTON

1900 TIMISOARA

Str. Samuil Micu nr.7

Telefon 96 - 18.35.25.

# INSTRUCTIUNILE Z80 SI DURATA LOR

## 1. Incarcari pe 8 biti

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| LD r,r' | 4 | 1 |
| LD r,n | 7 | 2 (4,3) |
| LD r,(HL) | 7 | 2 (4,3) |
| LD r,(IX+d) | 19 | 5 (4,4,3,5,3) |
| LD r,(IY+d) | 19 | 5 (4,4,3,5,3) |
| LD (HL),r | 7 | 2 (4,3) |
| LD (IX+d),r | 19 | 5 (4,4,3,5,3) |
| LD (IY+d),r | 19 | 5 (4,4,3,5,3) |
| LD (HL),n | 10 | 3 (4,3,3) |
| LD (IX+d),n | 19 | 5 (4,4,3,5,3) |
| LD (IY+d),n | 19 | 5 (4,4,3,5,3) |
| LD A,(BC) | 7 | 2 (4,3) |
| LD A,(DE) | 7 | 2 (4,3) |
| LD A,(nn) | 13 | 4 (4,3,3,3) |
| LD (BC),A | 7 | 2 (4,3) |
| LD (DE),A | 7 | 2 (4,3) |
| LD (nn),A | 13 | 4 (4,3,3,3) |
| LD A,I | 9 | 2 (4,5) |
| LD A,R | 9 | 2 (4,5) |
| LD I,A | 9 | 2 (4,5) |
| LD R,A | 9 | 2 (4,5) |

## 2. Incarcari pe 16 biti

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| LD rr,nn | 10 | 3 (4,3,3) |
| LD SP,nn | 10 | 3 (4,3,3) |
| LD IX,nn | 14 | 4 (4,4,3,3) |
| LD IY,nn | 14 | 4 (4,4,3,3) |
| LD HL,(nn) | 16 | 5 (4,3,3,3,3) |
| LD rr,(nn) | 20 | 6 (4,4,3,3,3,3) |
| LD SP,(nn) | 20 | 6 (4,4,3,3,3,3) |
| LD IX,(nn) | 20 | 6 (4,4,3,3,3,3) |
| LD IY,(nn) | 20 | 6 (4,4,3,3,3,3) |
| LD (nn),HL | 16 | 5 (4,3,3,3,3) |
| LD (nn),rr | 20 | 6 (4,4,3,3,3,3) |
| LD (nn),SP | 20 | 6 (4,4,3,3,3,3) |
| LD (nn),IX | 20 | 6 (4,4,3,3,3,3) |

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| LD (nn),IY | 20 | 6 (4,4,3,3,3,3) |
| LD SP,HL | 6 | 1 |
| LD SP,IX | 10 | 2 (4,6) |
| LD SP,IY | 10 | 2 (4,6) |
| PUSH rr | 11 | 3 (5,3,3) |
| PUSH IX | 15 | 4 (4,5,3,3) |
| PUSH IY | 15 | 4 (4,5,3,3) |
| POP rr | 10 | 3 (4,3,3) |
| POP IX | 14 | 4 (4,4,3,3) |
| POP IY | 14 | 4 (4,4,3,3) |

## 3. Schimb , transferuri in bloc si cautari

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| EX DE,HL | 4 | 1 |
| EX AF,AF' | 4 | 1 |
| EXX | 4 | 1 |
| EX (SP),HL | 19 | 5 (4,3,4,3,5) |
| EX (SP),IX | 23 | 6 (4,4,3,4,3,5) |
| EX (SP),IY | 23 | 6 (4,4,3,4,3,5) |
| LDI | 16 | 4 (4,4,3,5) |
| LDIR | 21 ptr. BC <> 0 | 5 (4,4,3,5,5) |
| | 16 ptr. BC = 0 | 4 (4,4,3,5) |
| LDD | 16 | 4 (4,4,3,5) |
| LDDR | 21 ptr. BC <> 0 | 5 (4,4,3,5,5) |
| | 16 ptr. BC = 0 | 4 (4,4,3,5) |
| CPI | 16 | 4 (4,4,3,5) |
| CPIR | 21 ptr. BC <> 0 | 5 (4,4,3,5,5) |
| | 16 ptr. BC = 0 | 4 (4,4,3,5) |
| CPD | 16 | 4 (4,4,3,5) |
| CPDR | 21 ptr. BC <> 0 | 5 (4,4,3,5,5) |
| | 16 ptr. BC = 0 | 4 (4,4,3,5) |

## 4. Operatii aritmetice si logice pe 8 biti

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| ADD A,r | 4 | 1 |
| ADD A,n | 7 | 2 (4,3) |
| ADD A,(HL) | 7 | 2 (4,3) |
| ADD A,(IX+d) | 19 | 5 (4,4,3,5,3) |
| ADD A,(IY+d) | 19 | 5 (4,4,3,5,3) |
| ADC A,r | 4 | 1 |
| ADC A,n | 7 | 2 (4,3) |

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| ADC A,(HL) | 7 | 2 (4,3) |
| ADC A (IX+d) | 19 | 5 (4,4,3,5,3) |
| ADC A,(IY+d) | 19 | 5 (4,4,3,5,3) |
| SUB r | 4 | 1 |
| SUB n | 7 | 2 (4,3) |
| SUB (HL) | 7 | 2 (4,3) |
| SUB (IX+d) | 19 | 5 (4,4,3,5,3) |
| SUB (IY+d) | 19 | 5 (4,4,3,5,3) |
| SBC A,r | 4 | 1 |
| SBC A,n | 7 | 2 (4,3) |
| SBC A,(HL) | 7 | 2 (4,3) |
| SBC A,(IX+d) | 19 | 5 (4,4,3,5,3) |
| SBC A,(IY+d) | 19 | 5 (4,4,3,5,3) |
| AND r | 4 | 1 |
| AND n | 7 | 2 (4,3) |
| AND (HL) | 7 | 2 (4,3) |
| AND (IX+d) | 19 | 5 (4,4,3,5,3) |
| AND (IY+d) | 19 | 5 (4,4,3,5,3) |
| OR r | 4 | 1 |
| OR n | 7 | 2 (4,3) |
| OR (HL) | 7 | 2 (4,3) |
| OR (IX+d) | 19 | 5 (4,4,3,5,3) |
| OR (IY+d) | 19 | 5 (4,4,3,5,3) |
| XOR r | 4 | 1 |
| XOR n | 7 | 2 (4,3) |
| XOR (HL) | 7 | 2 (4,3) |
| XOR (IX+d) | 19 | 5 (4,4,3,5,3) |
| XOR (IY+d) | 19 | 5 (4,4,3,5,3) |
| CP r | 4 | 1 |
| CP n | 7 | 2 (4,3) |
| CP (HL) | 7 | 2 (4,3) |
| CP (IX+d) | 19 | 5 (4,4,3,5,3) |
| CP (IY+d) | 19 | 5 (4,4,3,5,3) |
| INC r | 4 | 1 |
| INC (HL) | 11 | 3 (4,3,4) |
| INC (IX+d) | 23 | 6 (4,4,3,5,4,3) |
| INC (IY+d) | 23 | 6 (4,4,3,5,4,3) |
| DEC r | 4 | 1 |
| DEC (HL) | 11 | 3 (4,4,3) |
| DEC (IX+d) | 23 | 6 (4,4,3,5,4,3) |
| DEC (IY+d) | 23 | 6 (4,4,3,5,4,3) |

## 5. Instructiuni aritmetice de uz general si de control CPU

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| DAA | 4 | 1 |
| CPL | 4 | 1 |
| NEG | 8 | 2 (4,4) |

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| CCF | 4 | 1 |
| SCF | 4 | 1 |
| NOP | 4 | 1 |
| HALT | 4 | 1 |
| DI | 4 | 1 |
| EI | 4 | 1 |
| IM 0 | 8 | 2 (4,4) |
| IM 1 | 8 | 2 (4,4) |
| IM 2 | 8 | 2 (4,4) |

## 6. Instructiuni aritmetice pe 16 biti

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| ADD HL,rr | 11 | 3 (4,4,3) |
| ADD HL,SP | 11 | 3 (4,4,3) |
| ADC HL,rr | 15 | 4 (4,4,4,3) |
| ADC HL,SP | 15 | 4 (4,4,4,3) |
| SBC HL,rr | 15 | 4 (4,4,4,3) |
| SBC HL,SP | 15 | 4 (4,4,4,3) |
| ALD IX,BC | 15 | 4 (4,4,4,3) |
| ADD IX,DE | 15 | 4 (4,4,4,3) |
| ADD IX,IX | 15 | 4 (4,4,4,3) |
| ADD IX,SP | 15 | 4 (4,4,4,3) |
| ADD IY,BC | 15 | 4 (4,4,4,3) |
| ADD IY,DE | 15 | 4 (4,4,4,3) |
| ADD IY,IY | 15 | 4 (4,4,4,3) |
| ADD IY,SP | 15 | 4 (4,4,4,3) |
| INC rr | 6 | 1 |
| INC SP | 6 | 1 |
| INC IX | 10 | 2 (4,6) |
| INC IY | 10 | 2 (4,6) |
| DEC rr | 6 | 1 |
| DEC SP | 6 | 1 |
| DEC IX | 10 | 2 (4,6) |
| DEC IY | 10 | 2 (4,6) |

## 7. Rotatii si deplasari

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| RLCA | 4 | 1 |
| RLA | 4 | 1 |
| RRCA | 4 | 1 |
| RRA | 4 | 1 |

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| RLC r | 8 | 2 (4,4) |
| RLC (HL) | 15 | 4 (4,4,4,3) |
| RLC (IX+d) | 23 | 6 (4,4,3,5,4,3) |
| RLC (IY+d) | 23 | 6 (4,4,3,5,4,3) |
| RL r | 8 | 2 (4,4) |
| RL (HL) | 15 | 4 (4,4,4,3) |
| RL (IX+d) | 23 | 6 (4,4,3,5,4,3) |
| RL (IY+d) | 23 | 6 (4,4,3,5,4,3) |
| RRC r | 8 | 2 (4,4) |
| RRC (HL) | 15 | 4 (4,4,4,3) |
| RRC (IX+d) | 23 | 6 (4,4,3,5,4,3) |
| RRC (IY+d) | 23 | 6 (4,4,3,5,4,3) |
| SLA r | 8 | 2 (4,4) |
| SLA (HL) | 15 | 4 (4,4,4,3) |
| SLA (IX+d) | 23 | 6 (4,4,3,5,4,3) |
| SLA (IY+d) | 23 | 6 (4,4,3,5,4,3) |
| SRA r | 8 | 2 (4,4) |
| SRA (HL) | 15 | 4 (4,4,4,3) |
| SRA (IX+d) | 23 | 6 (4,4,3,5,4,3) |
| SRA (IY+d) | 23 | 6 (4,4,3,5,4,3) |
| SRL r | 8 | 2 (4,4) |
| SRL (HL) | 15 | 4 (4,4,4,3) |
| SRL (IX+d) | 23 | 6 (4,4,3,5,4,3 ) |
| SRL (IY+d) | 23 | 6 (4,4,3,5,4,3) |
| RLD | 18 | 5 (4,4,3,4,3) |
| RRD | 18 | 5 (4,4,3,4,3) |

## 8. Setari , resetari si teste de bit

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| BIT b,r | 8 | 2 (4,4) |
| BIT b,(HL) | 12 | 3 (4,4,4) |
| BIT b,(IX+d) | 20 | 5 (4,4,3,5,4) |
| BIT b,(IY+d) | 20 | 5 (4,4,3,5,4) |
| SET b,r | 8 | 2 (4,4) |
| SET b,(HL) | 15 | 4 (4,4,4,3) |
| SET b,(IX+d) | 23 | 6 (4,4,3,5,4,3) |
| SET b,(IY+d) | 23 | 6 (4,4,3,5,4,3) |
| RES b,r | 8 | 2 (4,4) |
| RES b,(HL) | 15 | 4 (4,4,4,3) |
| RES b,(IX+d) | 23 | 6 (4,4,3,5,4,3) |
| RES b,(IY+d) | 23 | 6 (4,4,3,5,4,3) |

## 9. Instructiuni de salt

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| JP nn | 10 | 3 (4,3,3) |
| JP cc,nn | 10 | 3 (4,3,3) |
| JR e | 12 | 3 (4,3,5) |
| JR C,e | 12 daca CY = 1 (salt) | 3 (4,3,5) |
| | 7 daca CY = 0 (cont) | 2 (4,3) |
| JR NC,e | 12 daca CY = 0 (salt) | 3 (4,3,5) |
| | 7 daca CY = 1 (cont) | 2 (4,3) |
| JR Z,e | 12 daca Z = 1 (salt) | 3 (4,3,5) |
| | 7 daca Z = 0 (cont) | 2 (4,3) |
| JR NZ,e | 12 daca Z = 0 (salt) | 3 (4,3,5) |
| | 7 daca Z = 1 (cont) | 2 (4,3) |
| JP (HL) | 4 | 1 |
| JP (IX) | 8 | 2 (4,4) |
| JP (IY) | 8 | 2 (4,4) |
| DJNZ e | 13 daca B <> 0 (salt) | 3 (5,3,5) |
| | 8 daca B = 0 (cont) | 2 (5,3) |

## 10. Apel de subrutine si intoarceri din subrutine

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| CALL nn | 17 | 5 (4,3,4,3,3) |
| CALL cc,nn | 17 in cazul apelului | 5 (4,3,4,3,3) |
| | 10 cind se continua , | 3 (4,3,3) |
| RET | 10 | 3 (4,3,3) |
| RET cc | 11 in cazul RET | 3 (5,3,3) |
| | 5 cind se continua | 1 |
| RETI | 14 | 4 (4,4,3,3) |
| RETN | 14 | 4 (4,4,3,3) |
| RST p | 11 | 3 (5,3,3) |

## 11. Instructiuni de intrare / iesire

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| IN A,(n) | 11 | 3 (4,3,4) |
| IN r,(C) | 12 | 3 (4,4,4) |
| INI | 16 | 4 (4,5,3,4) |
| INIR | 21 ptr. B <> 0 (rep.) | 5 (4,5,3,4,5) |
| | 16 ptr. B = 0 (cont.) | 4 (4,5,3,4) |

| INSTRUCTIUNEA | T-STATES | M-CYCLES |
|---|---|---|
| IND | 16 | 4 (4,5,3,4) |
| INDR | 21 ptr. B <> 0 (rep.)<br>16 ptr. B = 0 (cont.) | 5 (4,5,3,4,5)<br>4 (4,5,3,4) |
| OUT (n),A | 11 | 3 (4,3,4) |
| OUT (C),r | 12 | 3 (4,4,4) |
| OUTI | 16 | 4 (4,5,3,4) |
| OTIR | 21 ptr. B <> 0 (rep.)<br>16 ptr. B = 0 (cont.) | 5 (4,5,3,4,5)<br>4 (4,5,3,4) |
| OUTD | 16 | 4 (4,5,3,4) |
| OTDR | 21 ptr. B <> 0 (rep.)<br>16 ptr. B = 0 (cont.) | 5 (4,5,3,4,5)<br>4 (4,5,3,4) |

## INSTRUCTIUNILE Z80 GRUPATE DUPA VITEZA

### 1. Instructiuni care se executa in 4 T-states

1.1. Instructiuni de incarcare pe 8 biti :

```
LD   r,r'
```

1.2. Instructiuni de schimb :

```
EX   DE,HL
EX   AF,AF'
EXX
```

1.3. Instructiuni aritmetice si logice pe 8 biti :

```
ADD  A,r          OR   r
ADC  A,r          XOR  r
SUB  r            CP   r
SBC  A,r          INC  r
AND  r            DEC  r
```

1.4. Instructiuni aritmetice de uz general si control CPU :

```
DAA               NOP
CPL               HALT
CCF               DI
SCF               EI
```

1.5. Rotatii :

```
RLCA
RLA
RRCA
RRA
```

1.6. Instructiuni de salt :

```
JP    (HL)
```

## 2. Instructiuni care se executa in 5 T-states

2.1. Instructiuni de intoarcere conditionata din subrutine

```
RET  cc     > in cazul nerealizarii conditiei
              ( neexecutarii intoarcerii )
```

## 3. Instructiuni care se executa in 6 T-states

3.1. Instructiuni de incarcare pe 16 biti :

```
LD   SP,HL
```

3.2. Instructiuni aritmetice pe 16 biti :

```
INC  rr
INC  SP
DEC. rr
DEC  SP
```

## 4. Instructiuni care se executa in 7 T-states

4.1. Instructiuni de incarcare pe 8 biti :

```
LD   r,n              LD   A,(DE)
LD   r,(HL)           LD   (BC),A
LD   (HL),r           LD   (DE),A
LD   A,(BC)
```

4.2. Instructiuni aritmetice si logice pe 8 biti :

```
ADD  A,n              AND  n
ADD  A,(HL)           AND  (HL)
ADC  A,n              OR   n
ADC  A,(HL)           OR   (HL)
SUB  n                XOR  n
SUB  (HL)             XOR  (HL)
SBC  A,n              CP   n
SBC  A,(HL)           CP   (HL)
```

4.3. Instructiuni de salt conditionat :

```
JR   C,e      > cazul nerealizarii saltului
JR   NC,e     > cazul nerealizarii saltului
JR   Z,e      > cazul nerealizarii saltului
JR   NZ,e     > cazul nerealizarii saltului
```

## 5. Instructiuni care se executa in 8 T-states

### 5.1. Instructiuni aritmetice de uz general si control CPU :

```
NEG
IM   0
IM   1
IM   2
```

### 5.2. Rotatii si deplasari :

```
RLC  r          SLA  r
RL   r          SRA  r
RRC  r          SRL  r
```

### 5.3. Setari , resetari si teste de bit :

```
BIT  b,r
SET  b,r
RES  b,r
```

### 5.4. Instructiuni de salt :

```
JP    (IX)
JP    (IY)
DJNZ e        > cazul B = 0 (nerealizarea saltului)
```

## 6. Instructiuni care se executa in 9 T-states

### 6.1. Instructiuni de incarcare pe 8 biti :

```
LD   A,I
LD   A,R
LD   I,A
LD   R,A
```

## 7. Instructiuni care se executa in 10 T-states

### 7.1. Instructiuni de incarcare pe 8 biti :

```
LD   (HL),n
```

### 7.2. Instructiuni de incarcare pe 16 biti :

```
LD   rr,nn
LD   SP,nn
LD   SP,IX
LD   SP,IY
POP  rr
```

7.3. Instructiuni aritmetice pe 16 biti :

```
INC  IX
INC  IY
DEC  IX
DEC  IY
```

7.4. Instructiuni de salt :

```
JP   nn
JP   cc,nn    > indiferent de conditie
```

7.5. Instructiuni de apel de subrutine si intoarceri :

```
CALL cc,nn    > cazul nerealizarii conditiei
                ( nechemarii subrutinei )
RET
```

8. Instructiuni care se executa in 11 T-states

8.1. Instructiuni de incarcare pe 16 biti :

```
PUSH rr
```

8.2. Instructiuni aritmetice pe 8 biti :

```
INC  (HL)
DEC  (HL)
```

8.3. Instructiuni aritmetice pe 16 biti :

```
ADD  HL,rr
ADD  HL,SP
```

8.4. Instructiuni de apel de subrutine si intoarceri :

```
RST  p
RET  cc     > cazul indeplinirii conditiei
              ( realizarii intoarcerii )
```

8.5. Instructiuni de intrare / iesire :

```
IN   A,(n)
OUT  (n),A
```

9. Instructiuni care se executa in 12 T-states

9.1. Testari de bit :

```
BIT  b,(HL)
```

### 9.2. Instructiuni de salt :

```
JR   e
JR   C,e      > cazul CY = 1 ( realizarii saltului)
JR   NC,e     > cazul CY = 0 ( realizarii saltului)
JR   Z,e      > cazul Z = 1 ( realizarii saltului )
JR   NZ,e     > cazul Z = 0 ( realizarii saltului )
```

### 9.3. Instructiuni de intrare / iesire :

```
IN    r,(C)
OUT   (C),r
```

## 10. Instructiuni care se executa in 13 T-states

### 10.1. Instructiuni de incarcare pe 8 biti :

```
LD   A,(nn)
LD   (nn),A
```

### 10.2. Instructiuni de salt :

```
DJNZ e        > cazul B <> 0 ( realizarii saltului)
```

## 11. Instructiuni care se executa in 14 T-states

### 11.1. Instructiuni de incarcare pe 16 biti :

```
LD   IX,nn                    POP  IX
LD   IY,nn                    POP  IY
```

### 11.2. Instructiuni de intoarcere din subrutine :

```
RETI                          RETN
```

## 12. Instructiuni care se executa in 15 T-states

### 12.1 Instructiuni de incarcare pe 16 biti :

```
PUSH IX                       PUSH IY
```

### 12.2. Instructiuni aritmetice pe 16 biti :

```
ADC  HL,rr                    ADD  IX,IX
ADC  HL,SP                    ADD  IX,SP
SBC  HL,rr                    ADD  IY,BC
SBC  HL,SP                    ADD  IY,DE
ADD  IX,BC                    ADD  IY,IY
ADD  IX,DE                    ADD  IY,SP
```

12.3. Rotatii si deplasari :

```
RLC  (HL)                    SLA  (HL)
RL   (HL)                    SRA  (HL)
RRC  (HL)                    SRL  (HL)
```

12.4. Setari si resetari de biti :

```
SET  b,(HL)                  RES  b,(HL)
```

## 13. Instructiuni care se executa in 16 T-states

13.1. Instructiuni de incarcare pe 16 biti :

```
LD   HL,(nn)    LD   (nn),HL
```

13.2. Instructiuni de transfer in bloc si cautari :

```
LDI
LDD
CPI
CPD
LDIR        > cazul cind BC = 0 ( continue )
LDDR        > cazul cind BC = 0 ( continue )
CPIR        > cazul cind BC = 0 ( continue )
CPDR        > cazul cind BC = 0 ( continue )
```

13.3. Instructiuni de intrare / iesire :

```
INI
IND
OUTI
OUTD
INIR        > cazul cind B = 0 ( continue )
INDR        > cazul cind B = 0 ( continue )
OTIR        > cazul cind B = 0 ( continue )
OTDR        > cazul cind B = 0 ( continue )
```

## 14. Instructiuni care se executa in 17 T-states

14.1. Instructiuni de apel de subrutina :

```
CALL nn
CALL cc,nn     > cazul indeplinirii conditiei
                 ( realizarii apelului )
```

## 15. Instructiuni care se executa in 18 T-states

### 15.1. Rotatii :

```
RLD          RRD
```

## 16. Instructiuni care se executa in 19 T-states

### 16.1. Instructiuni de incarcare pe 8 biti :

```
LD   r,(IX+d)
LD   r,(IY+d)
LD   (IX+d),r
LD   (IY+d),r
LD   (IX+d),n
LD   (IY+d),n
```

### 16.2. Instructiuni de schimb :

```
EX   (SP),HL
```

### 16.3. Instructiuni aritmetice si logice pe 8 biti :

```
ADD  A,(IX+d)          AND  (IX+d)
ADD  A,(IY+d)          AND  (IY+d)
ADC  A,(IX+d)          OR   (IX+d)
ADC  A,(IY+d)          OR   (IY+d)
SUB  (IX+d)            XOR  (IX+d)
SUB  (IY+d)            XOR  (IY+d)
SBC  A,(IX+d)          CP   (IX+d)
SBC  A,(IY+d)          CP   (IY+d)
```

## 17. Instructiuni care se executa in 20 T-states

### 17.1. Instructiuni de incarcare pe 16 biti :

```
LD   rr,(nn)           LD   (nn),rr
LD   SP,(nn)           LD   (nn),SP
LD   IX,(nn)           LD   (nn),IX
LD   IY,(NN)           LD   (nn),IY
```

### 17.2. Testari de bit :

```
BIT  b,(IX+d)
BIT  b,(IY+d)
```

## 18. Instructiuni care se executa in 21 T-states

### 18.1. Transferuri in bloc si cautari :

```
LDIR          > cazul BC <> 0 ( repeat )
LDDR          > cazul BC <> 0 ( repeat )
CPIR          > cazul BC <> 0 ( repeat )
CPDR          > cazul BC <> 0 ( repeat )
```

### 18.2. Instructiuni de intrare / iesire :

```
INIR          > cazul B <> 0 ( repeat )
INDR          > cazul B <> 0 ( repeat )
OTIR          > cazul B <> 0 ( repeat )
OTDR          > cazul B <> 0 ( repeat )
```

## 19. Instructiuni care se executa in 23 T-states

### 19.1. Instructiuni de schimb :

```
EX   (SP),IX
EX   (SP),IY
```

### 19.2. Instructiuni aritmetice pe 8 biti :

```
INC  (IX+d)
INC  (IY+d)
DEC  (IX+d)
DEC  (IY+d)
```

### 19.3. Rotatii si deplasari :

```
RLC  (IX+d)          SLA  (IX+d)
RLC  (IY+d)          SLA  (IY+d)
RL   (IX+d)          SRA  (IX+d)
RL   (IY+d)          SRA  (IY+d)
RRC  (IX+d)          SRL  (IX+d)
RRC  (IY+d)          SRL  (IY+d)
```

### 19.4. Setari si resetari de biti :

```
SET  b,(IX+d)
SET  b,(IY+d)
RES  b,(IX+d)
RES  b,(IY+d)
```

**NOTA:** Pentru un sistem SPECTRUM (sau un calculator compatibil) la care procesorul are tactul de 3.54 MHz, duratele de executie a instructiunilor sint următoarele :

| Numarul de T-states | Timpul de executie [ microsecunde ] |
|---|---|
| 4 | 1.1299435 |
| 5 | 1.4124294 |
| 6 | 1.6949153 |
| 7 | 1.9774011 |
| 8 | 2.2598870 |
| 9 | 2.5423729 |
| 10 | 2.8248588 |
| 11 | 3.1073446 |
| 12 | 3.3898305 |
| 13 | 3.6723164 |
| 14 | 3.9548023 |
| 15 | 4.2372881 |
| 16 | 4.5197740 |
| 17 | 4.8022599 |
| 18 | 5.0847458 |
| 19 | 5.3672316 |
| 20 | 5.6497175 |
| 21 | 5.9322034 |
| 23 | 6.4971751 |

Va multumim cà ati cumpàrat manualul firmei noastre. Acest manual a fost editat si corectat cu toatà atentia si presupunem cà este corect (dar desigur perfectibil).

ALPHA Ltd. isi imbunàtàteste permanent manualele editate si de aceea và sintem recunoscàtori pentru orice sesizare. Và asteptàm cu orice problemà la sediul firmei si la tel.961/12936

**IMPORTANT !**

Edituta "TM" pune la dispozitia tuturor celor interesati întreaga gamă de manuale în limba română pentru calculatoare compatibile ZX Spectrum (TIM S, TIM S Plus, COBRA, HC 85, CIP, Jet) editate de firma "ALPHA Ltd" S.R.L. :

1.01 Limbajul BASIC pe întelesul tuturor în 12 lectii
1.02 Documentatie GENS și MONS (Asamblor-dezasamblor)
1.03 Documentatie limbaj FORTH
1.04 Documentatie BETA BASIC 3.1 (Extensie BASIC)
1.05 Documentatie BETA BASIC 3.1 (Rezumat)
1.06 Documentatie compilator FORTRAN 77-S
1.07 Documentatie editor de texte TASWORD
1.08 Documentatie compilator BLAST
1.09 Documentatie compilator PASCAL HP4TM (Rezumat)
1.10 Documentatie limbaj C
1.11 Memento timing cod mașină Z80
1.12 Documentatie MEGA BASIC (Extensie BASIC)
1.13 Documentatie VU-CALC
1.14 Manual BASIC avansati - conținînd și referiri la COBRA
1.15 Documentatie compilator COLT
1.16 Documentatie MASTER - FILE (sistem gestiune afaceri)
1.17 Documentatie limbaj microPROLOG
1.18 Documentatie limbaj PASCAL HP4TM
1.19 Documentatie sistem operare CP/M cu referire la calculatorul COBRA
1.20 Manual ROM SPECTRUM complet dezasamblat
1.21 Documentatie LASER GENIUS (pachet programe pentru lucrul în cod masină)
1.22 Cum să obtinem cît mai mult de la calculatorul nostru o carte cu programe si trucuri atît pentru începători cît si pentru avansati, în două variante:
 a) Numai cartea, cu o parte din figuri în text
 b) Cartea si o casetă demonstrativă, cu toate programele si figurile introduse
1.23 Construiți singuri 20 de montaje electronice interfațabile cu microcalculatorul Dvs